A Low Current GaAs Monolithic Image Rejection Downconverter for X-Band Broadcast Satellite Applications

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Abstract—**This paper describes the design, fabrication and performance of a fully integrated *X*-band monolithic image rejection downcoverter. The downconverter consists of a low noise amplifier, an image rejection mixer and an intermediate frequency amplifier. The downconverter receives RF signals between 11.7 and 12.3 GHz and converts them down to IF frequency between 1.0 and 1.6 GHz. A conversion gain of 46 ± 1 dB, a noise figure of less than 3.3 dB and an image rejection of more than 30 dB have been achieved over the RF frequency range. The chip size of the downconverter is 1.9 mm × 2.2 mm and its current dissipation is only 43 mA. Since the downconverter has sufficient image rejection due to an on-chip band-stop filter, it requires no off-chip circuits. Therefore, the use of this down-converter in *X*-band broadcast satellite applications will lead to a great reduction in size and current dissipation.**

I. Introduction

MICROWAVE and millimeter-wave frequency converters are widely used in consumer and military communication systems. In order to make these systems smaller, more reliable and producible, multi-function monolithic microwave integrated circuits (MMIC's) have been developed [1], [2]. To date, the main emphasis of MMIC development has been placed on active-function circuits such as amplifiers, mixers and oscillators. As a result, the size of the active-function circuits were drastically reduced. However, passive-function circuits such as filters have remained relatively large. Thus, in order to further reduce the size of the systems, it is essential to miniaturize and integrate passive-function circuits.

In *X*-band broadcast satellite (BS) receivers, large off-chip filters for the image rejection result in a significant size. For drastic size reduction of the receiver, it is necessary to realize an image rejection mixer requiring no off-chip circuits. There are two methods to build image rejection mixers. One is a phase-type image rejection mixer, and the other is a filter-type image rejection mixer [3]. Although several monolithic phase-type image rejection mixers have been reported [4], [5], they required off-chip IF quadrature combiners. Our approach is a monolithic filter-type image rejection mixer which consists of a novel band-stop filter and an FET mixer [6]. The filter has a bridged-tee circuit configuration and an image rejection of 30 dB. The size of the filter is approximately 0.5 mm^2.

In addition to small size, current dissipation is another important figure of merit in consumer applications. However, it has not been of great concern in MMIC designs. In order to reduce current dissipation and maintain reasonable linearity, the operation bias condition and gate width of each GaAs MESFET were carefully determined. The total current dissipation of the developed MMIC is only 43 mA. This current dissipation is at least one-half of that of commercially available hybrid circuit counterparts.

The design consideration of the monolithic image rejection downconverter is discussed in Section II. The fabrication and performance are described in Sections III and IV, respectively.

II. Design Consideration

Fig. 1 shows the functional block diagram of the *X*-band BS receiver. The developed monolithic image rejection downconverter is composed of an RF low noise amplifier (LNA), an image rejection mixer (IRM) consisting of a filter and an FET mixer, and an intermediate frequency amplifier (IFA). Since the gain of the LNA strongly affects the dynamic range of the receiver, it is necessary to carefully determine the gain of the LNA. From the measurement of two-tone third-order intermodulation (IM3) of a 280 μm gate width GaAs MESFET functioning as a mixer, it was found that the GaAs MESFET exhibited a sufficiently low output power level of IM3 for *X*-band BS applications even if the LNA had a gain of 30 dB. Since the goal of the total conversion gain was more than 40 dB, it was determined that the gains of the LNA and IFA should be about 20 dB and 25 dB, respectively. The individual circuits (LNA, IRM and IFA) are designed to have low input and output VSWR's to minimize unpredictable interactions between the circuits.

Manuscript received March 31, 1992, revised July 27, 1992.

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IEEE Log Number 9203716.

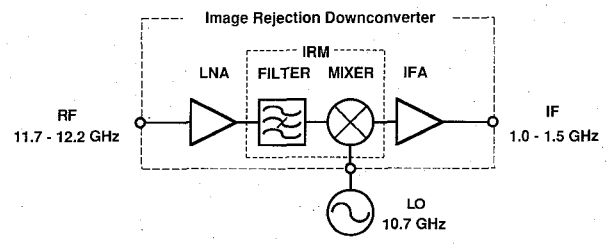

Fig. 1. Functional block diagram of the X-band broadcast satellite receiver.

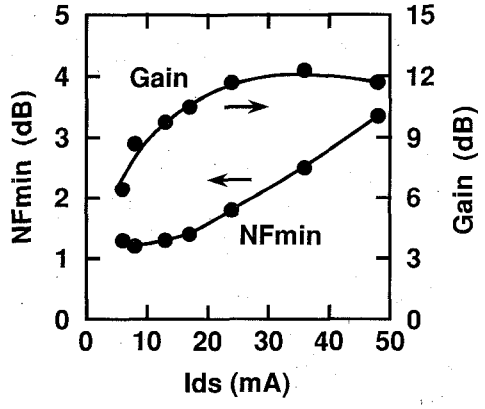

Fig. 2. The dependence of the noise figure and associated gain of a 280 μm gate width GaAs MESFET on the drain current.

TABLE I
COMPARISON OF PREDICTED LNA PERFORMANCE

	FET Performance			Predicted LNA Performance	
	Operation Current	NF	Gain	NF	Gain
One-stage LNA	20.0 mA	1.3 dB	11.0 dB	1.8 dB	10.0 dB
Two-stage LNA	10.0 mA	1.2 dB	9.0 dB	2.0 dB	17.0 dB
Three-stage LNA	6.7 mA	1.3 dB	6.5 dB	2.3 dB	18.5 dB

These circuits are then integrated on a single chip using a coplanar waveguide structure (CPW).

A. Low Noise Amplifier

In order to reduce the current dissipation and maintain an acceptable performance (noise figure and gain) of the LNA, it is important to carefully determine the operation bias condition of the GaAs MESFET. Thus, the dependence of the noise figure and associated gain of a 280 μm gate width GaAs MESFET on the drain current was measured with a drain operation voltage of 2 V, as shown in Fig. 2. The noise figure is almost constant at the drain current of 5 to 20 mA, and the associated gain increases as the drain current increases from 5 to 36 mA. Thus, an operation current of 20 mA optimally decreases the noise figure and increases the gain. At this bias condition, a one-stage LNA exhibiting a noise figure of 1.8 dB and a gain of 10 dB is predicted. However, in order to meet the gain requirement, a current dissipation of 40 mA is needed. To improve the performance of an LNA having a current dissipation of only 20 mA, the performance of a two-stage and three-stage LNA was calculated. The FET's in each LNA configuration are operated at the same current dissipation. The calculated results are shown in Table I. The two-stage and three-stage LNA's have almost the same performance and meet the gain requirement, however, the performance of the one-stage is considerably worse. Considering performance and chip size, the two-stage configuration was selected. The operation current of each FET was determined to be 10 mA.

Fig. 3 shows the circuit schematic of the LNA. Each stage includes a 0.3 μm $\times$ 280 μm GaAs MESFET. CPW transmission lines are used for impedance matching and metal-insulator-metal (MIM) capacitors are used for dc blocking and RF bypassing. Inductive series feedback in the first stage drives the optimum noise match closer to the optimum gain match [7]. In the second stage the inductive feedback is omitted in order to make the gain of the LNA higher. The input matching circuit of the first stage strongly affects the noise figure of the LNA. To re-

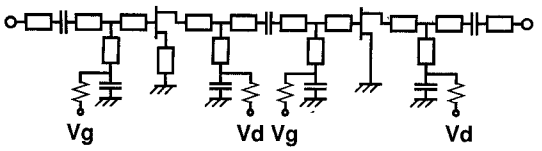

Fig. 3. Circuit schematic of the low noise amplifier.

duce the transmission loss of the CPW, 50 μm line width CPW is used in the input stage. The width of the CPW in the other stages is reduced to 10 μm to make the LNA smaller. It is predicted that the LNA has a gain of 17 dB and a noise figure of 2.0 dB with a drain voltage of 5 V and current dissipation of 20 mA. The size of the LNA is 50% smaller than that of the one reported previously [6]

B. Image Rejection Mixer

The key to the successful implementation of a monolithic image rejection downconverter is the design of an IRM requiring no off-chip circuits. The IRM reported here consists of a miniaturized band-stop filter and an FET mixer.

1. FILTER: In designing the monolithic filter, emphasis is placed on size reduction, sufficient image rejection and compatibility with MMIC fabrication technologies. Since the image rejection required in BS receivers in Japan is more than 31 dB, a filter must exhibit an image rejection of at least 25 dB, even if an LNA gives gain reduction in the image band. The solution proposed in this paper is a bridged-tee circuit incorporating a high-pass tee circuit and a bridged transmission line, as shown in Fig. 4. MIM capacitors are used in the tee circuit. The rejection frequencies (Fr) which define the stopband are calculated from $-Y_{21}/Y_{22} = 0$ as follows:

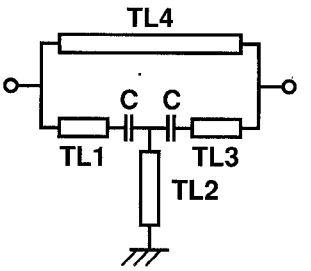

Fig. 4. Circuit schematic of the band-stop filter.

$$Fr = \frac{1}{2\pi}\sqrt{\frac{A1 + 2 \times A2 + A3 \pm \sqrt{(A1 - A3)^2 + 4 \times A2^2 - 4 \times A2 \times A4}}{2 \times C\sqrt{\epsilon\mu} \times (A1 \times A2 + A2 \times A3 + A3 \times A1 + A2 \times A4)}}$$

$$A1 = Z1 \times L1,\ A2 = Z2 \times L2,\ A3 = Z3 \times L3,\ A4 = Z4 \times L4$$

where $Z1$, $Z2$, $Z3$, $Z4$ and $L1$, $L2$, $L3$, $L4$ are the characteristic impedances and physical lengths of the transmission lines (TL's) 1, 2, 3, and 4, respectively. C is the capacitance in Fig. 4, and ϵ and μ are the permittivity and permeability of GaAs, respectively. When $Z1 = Z3$ and $L1 = L3$, the equation is simplified as follows:

$$Fr = \frac{1}{2\pi}\sqrt{\frac{A + A2 \pm \sqrt{A2 \times (A2 - A4)}}{C\sqrt{\epsilon\mu} \times (2 \times A \times A2 + A^2 + A2 \times A4)}}$$

$$A = Z1 \times L1 = Z3 \times L3.$$

The stopband and bandwidth are independently controllable with these parameters. In BS applications of our interest, the passband is 11.7 to 12.2 GHz, the local oscillator (LO) frequency is 10.7 GHz, and the stopband is 9.2 to 9.7 GHz. The filter circuit was optimized to obtain an image rejection of more than 25 dB and to be insensitive to the dispersion of the capacitances (C's in Fig. 4). The insertion loss at passband is predicted to be 2 dB. The cut-off frequency of the high-pass tee circuit is about 10 GHz and the characteristic impedance of all transmission lines is 50 Ω. The size of the filter is about 0.5 mm^2, which is much smaller than the other kinds of filters such as a quarter-wavelength coupled line filter.

2. FET Mixer: The FET mixer has a drain-local-injection configuration which does not require a combiner of RF and LO signals. Fig. 5 shows the circuit schematic of the mixer. The RF signal is applied to the gate, the LO signal is applied to the drain, and the IF signal is generated at the drain. The gate bias voltage is slightly above the pinch-off voltage, and the drain bias voltage is not applied. The GaAs MESFET size is 0.3 μm × 280 μm. In order to reduce the size of the mixer, all matching circuits are realized with lumped LC elements, including spiral inductors and MIM capacitors. Self-resonance of the spiral inductor ($L1$ in Fig. 5) is intentionally used to improve the LO-to-IF isolation and the LO injection efficiency. The mixer was designed using a harmonic balance simulator with a bias dependent GaAs MESFET model. The GaAs MESFET model parameters were extracted from both dc current-voltage characteristics and small signal S parameters. Great emphasis was placed on the agreement between measured and calculated data near the pinch-off voltage. The conversion gain of 0 dB is predicted from the simulation using the harmonic balance technique. The size of the mixer is 50% smaller than that of the one reported previously [6].

C. Intermediate Frequency Amplifier

Fig. 6 shows the circuit schematic of the IFA. The IFA consists of 6 FET's, 14 resistors, and 9 MIM capacitors. Spiral inductors were not used in order to reduce the size of the IFA. The IFA has four gain stages with input and output active matching stages, which are a common gate FET and a source follower, respectively. These active matching stages reduce the chip size and do not require large current dissipation. Each gain stage includes a com-

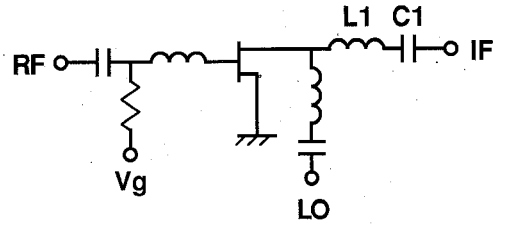

Fig. 5. Circuit schematic of the FET mixer.

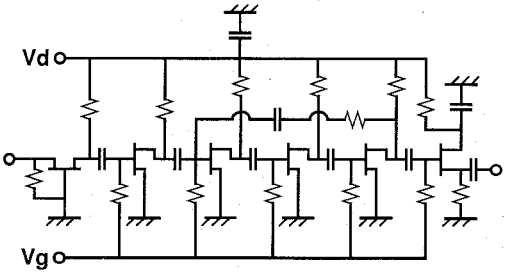

Fig. 6. Circuit schematic of the intermediate frequency amplifier.

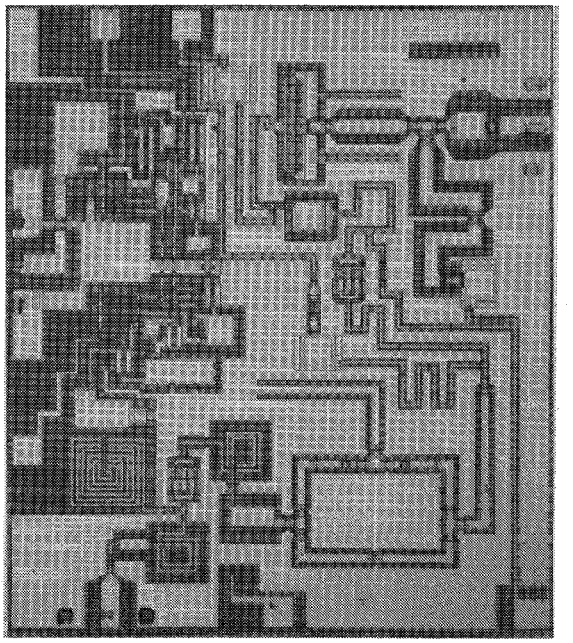

Fig. 7. Photograph of the monolithic image rejection downconverter.

mon source FET and a resistive load. Resistive feedback is used for flattening the gain of the IFA. In order to predict the linearity and current dissipation of the IFA, the large signal GaAs MESFET model parameters were extracted with emphasis on the agreement in the saturated region of current-voltage characteristics. Using a harmonic balance simulator, the gate width of each GaAs MESFET was optimized to achieve acceptable linearity and to reduce the current dissipation. The total gate width of the IFA is 680 μm. The IFA gain is predicted to be 30 dB with a drain bias voltage of 5 V and a current dissipation of 20 mA. The IFA size is 60% smaller than the one reported previously [6].

D. Image Rejection Downconverter

Since the individual circuits (LNA, IRM, IFA) are designed for a 50 Ω system, the image rejection downconverter is formed by simply connecting the individual circuits. A total conversion gain of 45 dB is predicted. The drain voltage is 5 V and the total current dissipation is predicted to be 40 mA. By decreasing the size of the matching circuits, the size of the image rejection downconverter was reduced to 1.9 mm × 2.2 mm, which was one-half of the size of the one reported previously.

III. Fabrication

An electron beam direct writing system was used to define all resist patterns. This system is effective in reducing the MMIC development period because it replaces the need for photo-masks, making it easy to modify the circuit layout. The GaAs MESFET has a 0.3 μm gate length and a 1.0 μm spacing between the source and drain n^+ regions. The channel of the GaAs MESFET's and n^+ layers were formed by Si implantation and were activated by using rapid thermal annealing. The ohmic and Schottky contacts were formed using AuGe/Ni/Au and Al, respectively. For the insulator of MIM capacitors, a 2000Å layer of Silicon nitride was deposited. The top metal was defined using an airbridge process in order to reduce crossover capacitances, and there was no backside processing. Fig. 7 shows a photograph of the image rejection downconverter chip. The chip size is 1.9 mm × 2.2 mm.

IV. RF Performance

The monolithic image rejection downconverter has been fully tested on wafer with an external local oscillator at 10.7 GHz. The drain voltage of the LNA and IFA is 5 V, and no drain bias is applied to the FET mixer. The current dissipation of the LNA and IFA is 22 mA and 21 mA, respectively, and the IRM consumes no dc current. The gate bias voltage of the FET mixer is slightly above the pinch-off voltage.

Fig. 8 shows the measured conversion gain and noise figure of the image rejection downconverter. The local oscillator power is 8 dBm. A conversion gain of 46 ± 1 dB and a noise figure of less than 3.3 dB have been achieved over the RF frequency range from 11.7 to 12.3 GHz. Fig. 9 illustrates the measured conversion gain and noise figure as a function of the local oscillator power. The RF frequency is fixed at 12.0 GHz. Conversion gain increases as the local oscillator power increases from −2 dBm to 10 dBm. The noise figure is almost constant at the local oscillator power of 8 to 12 dBm. The measured image rejection is shown in Fig. 10. The downconverter has exhibited an image rejection of 30 to 40 dB. The measured return loss at the RF and IF ports is shown in Fig. 11. The return loss at the RF port is more than 14 dB, and that at the IF port is more than 13 dB. Fig. 12 shows measured two-tone IM3 characteristics. The local oscil-

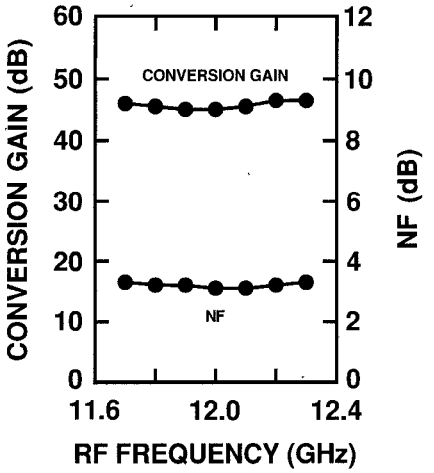

Fig. 8. Measured conversion gain and noise figure of the monolithic image rejection downconverter.

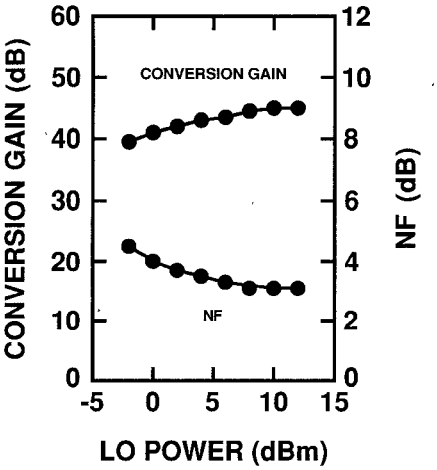

Fig. 9. Measured conversion gain and noise figure of the monolithic image rejection downconverter as a function of the local oscillator power.

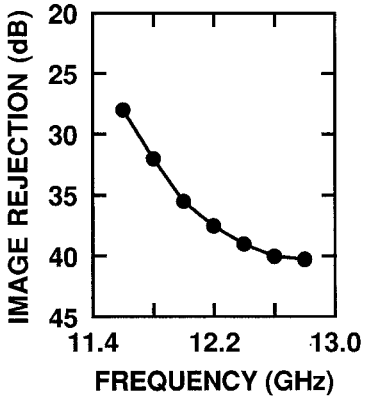

Fig. 10. Measured image rejection of the monolithic image rejection downconverter.

lator power was fixed at 8 dBm. The frequencies of the input signals are 12.0 GHz and 12.02 GHz. It is determined that the third-order intermodulation intercept point at the output is 11 dBm. The LO-to-RF and LO-to-IF isolations are 47 dB and 48 dB, respectively.

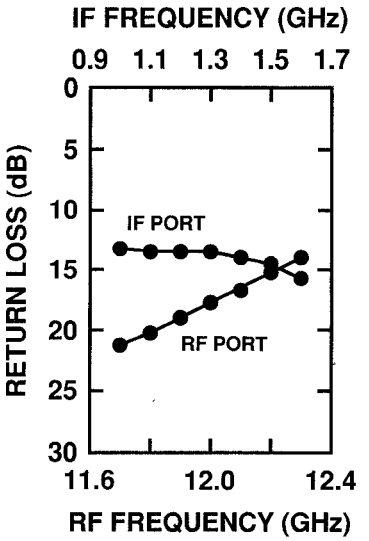

Fig. 11. Measured return loss at the RF and IF ports of the monolithic image rejection downconverter.

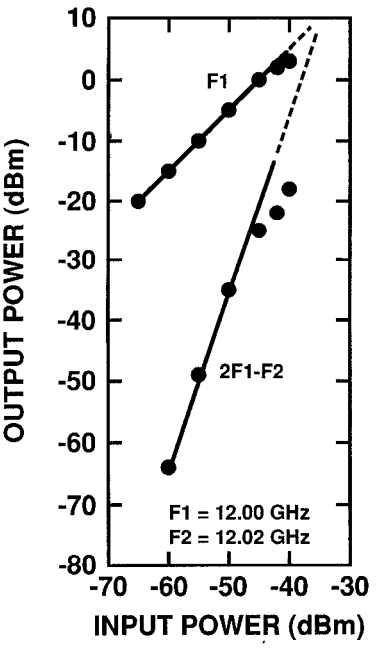

Fig. 12. Measured two-tone third-order intermodulation of the monolithic image rejection downconverter.

V. Conclusion

A monolithic image rejection downconverter has been designed, fabricated and fully tested for *X*-band BS applications. A conversion gain of 46 ± 1 dB and a noise figure of less than 3.3 dB have been achieved over the RF frequency range. Current dissipation of the downconverter is less than one-half of that of commercially available hybrid counterparts. Moreover, since the downconverter has an image rejection of more than 30 dB, a large off-chip filter is not needed in the receiver. Therefore, the developed downconverter could drastically reduce the size and current dissipation of BS receivers.

ACKNOWLEDGMENT

The authors wish to thank Prof. M. Maeda, Dr. N. Hashizume and Mr. T. Sakurai for their continued discussions and encouragement. They also would like to thank Mr. Y. Nakagawa and Dr. S. Hara for their helpful discussions, Mr. M. Isobe for setting up the CAD system, and Ms. M. Furukawa for RF measurements.

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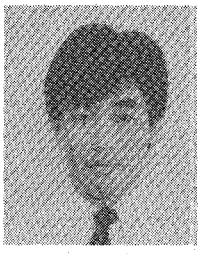

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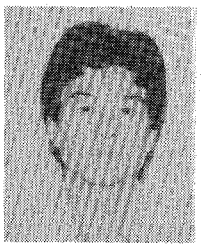

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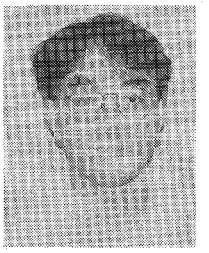

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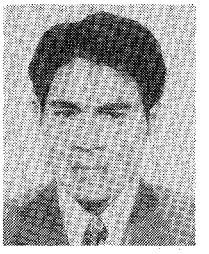

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